# **ELL304 Lab Report**

# **Laboratory 1: Device characterization**

**Name:** Anirudh Garg **Entry Number:**2020EE10469 **Lab Partner:** Geetigya Joshi

Aim: To get acquainted with MOS Devices

Apparatus Required:

1. CD4007 IC (Integrated Circuit)

2. Breadboard

3. 3-n Channel MOS Devices

4. 3-p Channel MOS Devices

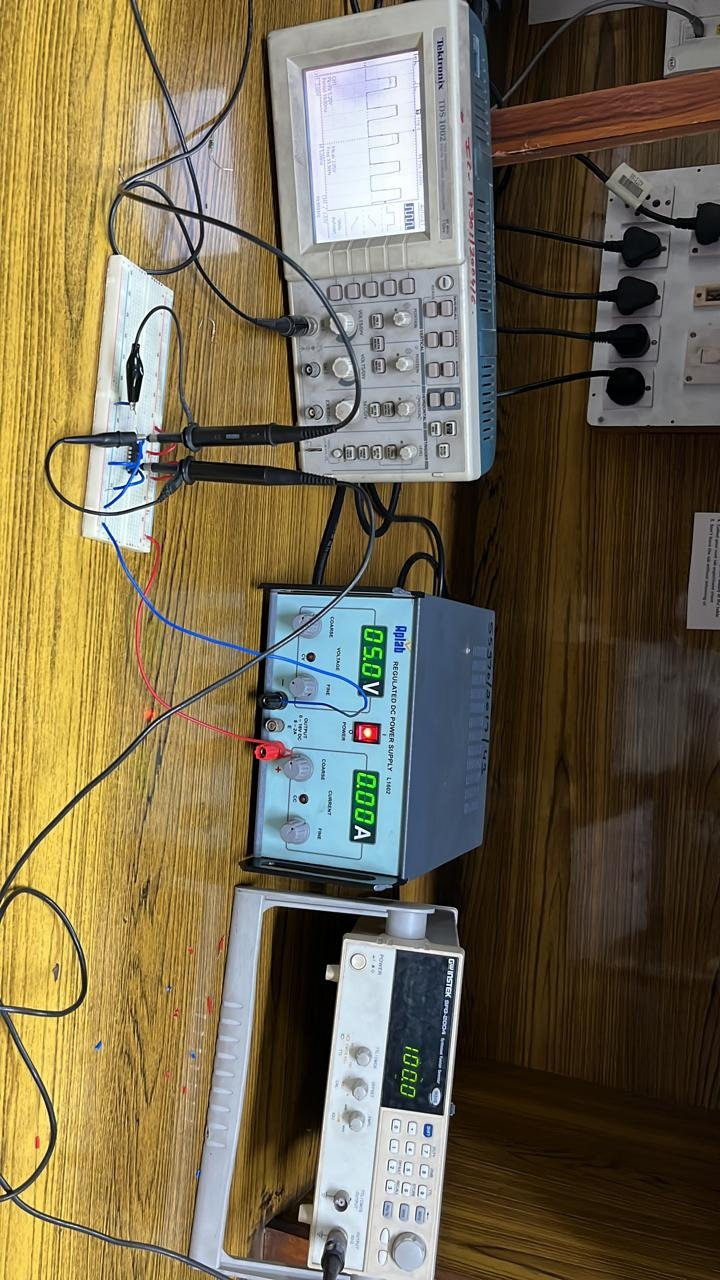
5. Various Resistances (220 Ω ,330 Ω, 1KΩ, 3.3 KΩ etc.)

6. Digital Storage Oscilloscope

7. Regulated Power Supply

8. Function Generator

9. Probes and Cables

Diagram, schematic

Description automatically generated

Procedure and Theory:

1. **Procedure:**

We must measure the value of Id for different values of Vgs using MN-1(N-MOS). Vgs of the circuit is controlled by using variety of values of R1. For this experiment, the drain and gate are connected.

Diagram, schematic

Description automatically generated

**Theory:**

The charge passing through a small cross-section of the channel is Q.v which gives I= Q.v

Using v= -*μnE,* and similarly integrating using E=-dV/dx; we get the equation

***Id* =1/2*μnCox W/L[*2(*VGS* – *VTH*)*VDS* – *VDS* 2]**

***Id* varies linearly with respect to Vgs as posed in theory.**

First, the linear dependence of *Id* upon *μn*,*Cox*, and *W/L* is to be expected: a higher mobility yields a greater current for a given drain-source voltage; a higher gate oxide capacitance leads to a larger electron density in the channel for a given gate-source voltage; and a larger *W/L .* Second, for a constant *VGS*, *Id* varies *parabolically* with *Vds* reaching a maximum of

***Id,max* =1/2*μnCox W/L*(*VGS* - *VTH*)2** and remaining constant thereafter.

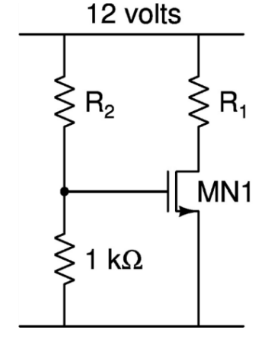
Diagram

Description automatically generated Diagram, schematic

Description automatically generated

1. **Procedure:**

**In this** we have to measure the Id vs Vds for the device MN1 varying values of Vgs. We have to fix the resistance R1 and vary R2 with values 470, 1k, 3k, 4.7k, 10k.The circuit is as given below:



**Theory:**

***Id* =1/2*μnCox W/L[*2(*VGS* – *VTH*)*VDS* – *VDS* 2]**

The above formula is valid for the triode region i.e., the region for which Vds<Vgs-Vth, after that the parabolic behaviour of the equation doesn’t hold as the length of pinch-off region decreases and is evaluated up to VGS - VTH rather than VDS. At the saturation region the formula is:

Text

Description automatically generated with low confidence

Diagram

Description automatically generated

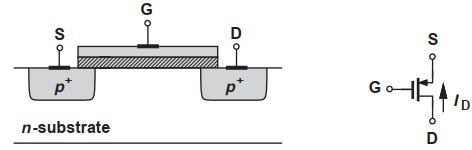
1. **Procedure:**

We must measure the value of Id for different values of Vgs using MN-1(N-MOS). Vgs of the circuit is controlled by using variety of values of R1. For this experiment, the drain and gate are connected.

**Secondly,** we also must measure the Id vs Vds for the device MN1 varying values of Vgs. We must fix the resistance R1 and vary R2 with values 470, 1k, 3k, 4.7k, 10k.

**Theory:**

For the P-MOS circuit, If the gate voltage is one threshold voltage lower than the source potential, the channel is now made up of holes. So, to turn on the device, Vgs must be greater than Vth, where Vth is negative.



The formulae for P-MOS are quite like N-MOS for triode and saturation region given as:

 A picture containing text

Description automatically generated

Mobility of holes is less than electrons, therefore PMOS devices exhibit a poorer performance than NMOS transistors.

1. **Procedure:**

Both the MN3 and MP3 devices are set up as a CMOS inverter. We have to vary Gate voltages, and the drain voltages are logged. Then using the triangle wave of the function generator, we must apply the different voltages.

**Theory:**

The working of CMOS inverter is the same as other types of FETs except depends on an oxygen layer to divide electrons within the gate & semiconductor. They are designed with a power supply, input voltage terminal, output voltage, gate, drain, and PMOS & NMOS transistors which are connected to the gate & the drain terminals.

When the low input voltage is given to the CMOS inverter, then the PMOS transistor is switched ON whereas the NMOS transistor will switch OFF by allowing the flow of electrons throughout the gate terminal & generating high logic output voltage.

Similarly, when the high input voltage is given to the CMOS inverter then, the PMOS transistor is switched OFF whereas the NMOS transistor will be switched ON avoiding as many electrons as possible from attaining the output voltage & generating low logic output voltage.

Thus, direct current supplies from the supply voltage (VDD) to the output voltage (Vout) & the load capacitor (CL) can be charged and shows that Vout = VDD. As a result, the above circuit works like an inverter.

